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# STIC EIC 2100 Search Request Form

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|---|---|
| Today's Date: 9/13/04 | What date would you like to use to limit the search? Priority Date: 12/28/01 Other: |

| | |
|---|---|
| Name Muhammad Ali | Format for Search Results (Circle One): PAPER DISK EMAIL |
| AU 2177 Examiner # 78414 | Where have you searched so far? |
| Room # 4Y18 Phone 605-4356 | USP DWPI EPO JPO ACM IBM TDB |
| Serial # 10/039,725 | IEEE INSPEC SPI Other ________ |

**Is this a "Fast & Focused" Search Request? (Circle One) YES NO**
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Analyzing & processing hierarchical data structures as a directed graphs which includes tree's & other non-cyclic graphs.

"Binding same graph$ same node$ same generate same object$ same pair$ same sub-node same set$"

"Node$ same relationship same graph same valid same sub-node same pattern$"

"Graph same logic"

STIC Searcher Terese Esterheld Phone 308-7795
Date picked up 9/13/04 10:20am Date Completed 9/13/04 1:30pm

sira Search and Information Resources Administration

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Set      Items   Description
S1      165358   (GRAPH? OR TABLE? OR TUPLE? OR ARRAY? OR MATRIX OR MATRICES
                  OR COLUMN? OR ROW? OR GRID? OR LINE? OR LABEL? OR VALUE? OR -
                 FAT OR MFAT OR NTFS OR VFAT OR (MATHEMATICAL OR DATA)()ELEMEN-
                 T?)(2N)(INFORMATION OR DATA)
S2      655336   NODE? OR TREE? OR SERVER? OR PROCESSOR?
S3       72218   (PAIR OR TWO OR COUPLE OR DUO OR DUAL OR DOUBLE)(2N)(PATTE-
                 RN? OR STRUCTURE? OR MODEL? OR PARAMETER? OR ATTRIBUT? OR FEA-
                 TURE?)
S4      956758   TARGET? OR OBJECT? OR GOAL? OR DESTINATION?
S5      372611   SUBNODE? OR SUB()NODE? OR SUBTREE? OR SUB()TREE? OR CHILD?
                 OR SIBLING? OR OFFSPRING OR OFF()SPRING OR BRANCH? OR LEAVES -
                 OR SLAVE?
S6         116   NODE()RELATIONSHIP()GRAPH? OR NRG
S7       31315   (WALK? OR TEST? ? OR TESTING OR DIAGNOSTIC OR ANALYS? OR A-
                 NALYZ? OR MEASURE? OR INSPECT? OR CHECK? OR VERIFY? OR EXAMIN?
                  OR EVALUAT? OR DETECT?)(2N)(ALGORITHM? OR RULE? OR FORMULA? -
                 OR LOGIC OR EXPRESSION? OR SCHEME? OR TECHNIQUE?)
S8           0   S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7
S9           3   S6 AND S7
S10          2   S1 AND S2 AND S3 AND S4 AND S5
S11         18   S1 AND S3 AND S5
S12         21   S9 OR S10 OR S11
S13         11   S12 AND IC=G06F?
File 347:JAPIO Nov 1976-2004/May(Updated 040903)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200458
         (c) 2004  Thomson Derwent
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016088163 **Image available**
WPI Acc No: 2004-246038/200423
Related WPI Acc No: 2003-800352
XRPX Acc No: N04-195058

**Data storing method for computer, by portioning** nodes **not yet assigned to hierarchical** tree **into outside and inside** child nodes **based on the comparison between the discriminator key and the segment data for a** node **under analysis**

Patent Assignee: CADENCE DESIGN SYSTEMS INC (CADE-N)
Inventor: KRONMILLER T; TEIG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6701306 | B1 | 20040302 | US 2000526266 | A | 20000315 | 200423 | B |
| | | | US 2001298135 | P | 20010612 | | |
| | | | US 200261447 | A | 20020131 | | |

Priority Applications (No Type Date): US 2001298135 P 20010612; US 2000526266 A 20000315; US 200261447 A 20020131
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6701306 | B1 | | 34 | G06F-017/30 | CIP of application US 2000526266 |
| | | | | | Provisional application US 2001298135 |
| | | | | | CIP of patent US 6625611 |

Abstract (Basic): US 6701306 B1

NOVELTY - **Nodes** not yet assigned to the hierarchical **tree** are then portioned into outside and inside **child** **nodes** based on the comparison between the discriminator key and the segment data for a **node** under analysis, and recursively portioning the **nodes** into the outside and inside **child** **nodes** for each level of the **tree** .

DETAILED DESCRIPTION - Segment data are generated for each n-sided geometric **object** , after which a hierarchical **tree** is generated, the **tree** having levels of **nodes** to represent the **objects** , with each **node** associated with a segment data. A discriminating **node** is then selected as a parent **node** , after which a discriminator dimension is computed. Vertices are then selected based on the computed dimension.

An INDEPENDENT CLAIM is also included for a computer readable medium.

USE - For computer. Also applicable for electronic design automation.

ADVANTAGE - Creates mechanisms to manipulate and store polygons in a multidimensional space.

DESCRIPTION OF DRAWING(S) - The figure illustrates the manner by which data relating to interconnect lines are stored on an integrated circuit.

**Two** -layer data **structure** (900)
Two-dimensional **array** of tile **data** structures (905)
Tile data structures (910)
Ng **tree** (915)
Pointers (920,925)
pp; 34 DwgNo 10/29

Title Terms: DATA; STORAGE; METHOD; COMPUTER; PORTION; **NODE** ; ASSIGN; HIERARCHY; **TREE** ; **CHILD** ; **NODE** ; BASED; COMPARE; DISCRIMINATE; KEY; SEGMENT; DATA; **NODE** ; ANALYSE
Derwent Class: T01
International Patent Class (Main): **G06F-017/30**
File Segment: EPI

**13/5/5 (Item 2 from file: 350)**

015494788 **Image available**
WPI Acc No: 2003-556935/200352
XRPX Acc No: N03-442569

**Non-cyclic electronic data graph analysis system, determines if target sub-node patterns for specific node pattern matches with valid sub-node patterns for corresponding node in** node relationship graph

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: CLEWIS F T; SITZE R A
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20030084054 | A1 | 20030501 | US 200139725 | A | 20011026 | 200352 | B |

Priority Applications (No Type Date): US 200139725 A 20011026
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20030084054 | A1 | | 17 | G06F-007/00 | |


Abstract (Basic): US 20030084054 A1

NOVELTY - Each node in a **node relationship graph** ( **NRG** ) (59) including computed valid sub-node patterns corresponds to a node in electronic data graph. An **analysis logic** (68) systematically **analyses** through nodes in the data graph and **NRG** . A testing system (72) determines if target sub-node patterns for a node pattern matches with valid sub-node patterns for corresponding **NRG** node when a node is encountered in the data graph.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) system for optimizing electronic data graph analysis;

(2) method for analyzing graph of hierarchical data; and

(3) computer program product for optimizing electronic data graph analysis.

USE - For collection, processing and analysis of hierarchical data structure including electronic information stored in databases for providing business intelligence, revealing consumer interests and determining marketplace trends to efficiently deliver goods and services to consumers.

ADVANTAGE - Allows multiple analysis tools to process directed non-cyclic data graph in parallel, thus efficiently eliminating the processing of unnecessary data, thereby efficient analysis of electronic information in database is enabled.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the electronic data graph analysis system.

**node relationship graph** (59)

**analysis logic** (68)

testing system (72)

pp; 17 DwgNo 3/8


Title Terms: NON; CYCLIC; ELECTRONIC; DATA; GRAPH; ANALYSE; SYSTEM; DETERMINE; TARGET; SUB; NODE; PATTERN; SPECIFIC; NODE; PATTERN; MATCH; VALID; SUB; NODE; PATTERN; CORRESPOND; NODE; NODE; RELATED; GRAPH
Derwent Class: T01
International Patent Class (Main): **G06F-007/00**
File Segment: EPI

**13/5/6 (Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


015369642
WPI Acc No: 2003-430580/200340
XRAM Acc No: C03-113945
XRPX Acc No: N03-343694

**Directing the synthesis of a combinatorial library of oligomers, useful for permitting complex genetic analyses to be carried out, comprises using encoded carrier support systems**

Patent Assignee: NANOMICS BIOSYSTEMS PTY LTD (NANO-N); BATTERSBY B J

readable data to provide a sum of the index values corresponding to a potency value for the compound(s); and

(f) an output hardware coupled to the central processing unit, for receiving the potency value.

ACTIVITY - Antiinflammatory.

SIGMAIV provides a potency of agent (PA), where 20-acetyl-ingenol-3 angelate exhibits a PA=SIGMAIV=15.

MECHANISM OF ACTION - protein kinase C(PKC) modulator.

USE - For the treatment or prophylaxis of an inflammatory condition (claimed). The composition can further be useful for treating pathogenic infections.

pp; 172 DwgNo 0/21

Title Terms: TREAT; PROPHYLACTIC; INFLAMMATION; CONDITION; COMPRISE; ADMINISTER; SYMPTOM; AMELIORATE; AMOUNT; CHEMICAL; AGENT; OBTAIN; PLANT; FAMILY
Derwent Class: B05; T01
International Patent Class (Main): A61K-031/66; A61K-035/78
International Patent Class (Additional): A61K-031/22; A61K-031/40; A61K-031/435; A61K-031/455; A61K-047/18; A61K-047/22; A61P-029/00; A61P-031/02; A61P-031/04; A61P-031/12; A61P-031/14; A61P-031/16; A61P-031/18; A61P-031/20; A61P-031/22; A61P-033/00; A61P-037/04; A61P-043/00; **G06F-019/00**
File Segment: CPI; EPI

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**13/5/8 (Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


012470480 **Image available**
WPI Acc No: 1999-276588/199923
XRPX Acc No: N99-207332

**Tree structured graphical visualisation method for cluster hierarchies of documents through user interaction - involves displaying nodes and** data elements **grouped in particular combinations in graphical tree** structures **in** two **modes of operation**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC )
Inventor: MAAREK Y S; VORTMAN P; WECKER A J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5895474 | A | 19990420 | US 96706937 | A | 19960903 | 199923 | B |

Priority Applications (No Type Date): GB 9517988 A 19950904
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5895474 | A | | 13 | G06F-017/00 | |

Abstract (Basic): US 5895474 A

NOVELTY - In one mode of operation, the visualization aid displays a graphical tree structure that includes a selected node and all **branches** of selected node, including all sub-ordinate nodes and **data elements** . In the other mode, a single group of all **data elements** is displayed. DETAILED DESCRIPTION - The graphical tree structure displayed in one mode, includes all **data elements branches** directly from the selected node, or directly from sub-ordinate nodes. In the other node, tree structure displayed includes the single group of all **data elements branches** either directly from selected or sub-ordinate nodes, but the selected and its sub- ordinate are not displayed.

USE - As graphical visualization aid for digitally stored collection of **data elements** such as documents, programs and other data files.

ADVANTAGE - Enables user to interpret underlying structure in dendrogram, without burdening user with too much information and without cluttering up display screen. DESCRIPTION OF DRAWING(S) - The drawing shows the main steps in the tree structured graphical

visualization method.
Dwg.2/8
Title Terms: TREE; STRUCTURE; GRAPHICAL; VISUAL; METHOD; CLUSTER; DOCUMENT; THROUGH; USER; INTERACT; DISPLAY; NODE; DATA; ELEMENT; GROUP; COMBINATION ; GRAPHICAL; TREE; STRUCTURE; TWO; MODE; OPERATE
Derwent Class: T01
International Patent Class (Main): **G06F-017/00**
File Segment: EPI

**13/5/9 (Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


011631372 **Image available**
WPI Acc No: 1998-048500/199805
Related WPI Acc No: 2003-727345
XRPX Acc No: N98-038771
**Information** processor **using** object **network - has motion control system to** couple **various** models **based on data group which is controlled by database management system and carries out processing by checking given constraint**
Patent Assignee: FUJITSU LTD (FUIT )
Inventor: ENOMOTO H
Number of Countries: 002 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 9297684 | A | 19971118 | JP 9729457 | A | 19970213 | 199805 | B |
| US 5895459 | A | 19990420 | US 97810671 | A | 19970303 | 199923 | |

Priority Applications (No Type Date): JP 9646980 A 19960305
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 9297684 | A | | 29 | G06F-009/44 | |
| US 5895459 | A | | | G06F-015/00 | |

Abstract (Basic): JP 9297684 A
The **processor** uses an **object** network for processing an **information** using a **graphical** interface. The **data** and its processing are treated as an **object** in the network. The **object** model divides the attribute value structure in a hierarchical manner of each **object** to obtain the attribute values of a formal model and a characteristic model based on the template format of the **data** model. A **graphical** expression is obtained by using a noun **object** in a **node** and a verb **object** in a **branch** .

The function of the verb **object** are used to operate on the noun **object** . A DMS (50) controls the data group which stimulate the hierarchy of a system using the relationship between the process models corresponding to the **object** network. Based on the data group controlled by the DMS, a motion control system couples the models and carries out processing by checking the given constraint.

USE/ADVANTAGE - In language processing system, image processing system. Enables to develop systems efficiently. Enables to carry out constraint realisation of cooperation process as whole system. Enables to attain complicated service using simple method.
Dwg.1/29
Title Terms: INFORMATION; **PROCESSOR** ; **OBJECT** ; NETWORK; MOTION; CONTROL; SYSTEM; COUPLE; VARIOUS; MODEL; BASED; DATA; GROUP; CONTROL; DATABASE; MANAGEMENT; SYSTEM; CARRY; PROCESS; CHECK; CONSTRAIN
Index Terms/Additional Words: **DMSInform ation**
Derwent Class: T01
International Patent Class (Main): **G06F-009/44 ; G06F-015/00**
File Segment: EPI

**13/5/10 (Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

007243968
WPI Acc No: 1987-240975/198734
XRPX Acc No: N87-180115

**Network characteristics determn. unit - has topology modelling unit stopping analysis of** branches **after decoder signal passes through operational unit field**

Patent Assignee: AS UKR POWER MODELL (AUPO-R)
Inventor: DODONOV A G; MINCHENKO L I; PELEKHOV S P
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| SU 1282151 | A | 19870107 | SU 3806351 | A | 19841025 | 198734 | B |

Priority Applications (No Type Date): SU 3806351 A 19841025
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| SU 1282151 | A | | 13 | | |

Abstract (Basic): SU 1282151 A

Appts. comprises completed events numbers memory (31), number of **branches** input memory (32), subtractor (33), registers (34-36), final section number register (37), zero state decoder (38), codes comparator (39), commutators (40,41), triggers (42,43,52), AND-gates (44-51), OR-gate (53), NOT-gate (54), delay elements (55-58), all forming the operational unit (1), plus topology modelling unit (2), characteristics calculator (3) and clock oscillator (4). Speed is increased by the introduction to the topology **modelling** unit of **two** commutators, initial unit number register and delay element.

Initial **grid** topology **data** is first entered in memory elements along with records of **branches**.. Another memory receives width or duration codes plus the number of **branchey** entered in a given node.

A start signal is applied from an input field to the topology modelling unit and logic switching is carried out to enable reading of the first **branch** from a memory and a zero code corresp. to an earlier completed event.

The read-out value code passes to a register and subtractor (33) reduces the number of **Branches** held in memory (32) by one. The difference code formed passes to register (34) along with a control pulse and if the code is greater than zero, this indicates that not all **branches** have been analysed and that the operational unit has not executed any operations for a particular control pulse. Control pulse shaping is then blocked.

USE/ADVANTAGE - Appts. is esp. for specialised data processes in e.g. specialised computers for modelling operational control set tasks. Bul.1/7.1.87

Dwg.1/3

Title Terms: NETWORK; CHARACTERISTIC; DETERMINE; UNIT; TOPOLOGICAL; MODEL; UNIT; STOP; ANALYSE; **BRANCH** ; AFTER; DECODE; SIGNAL; PASS; THROUGH; OPERATE; UNIT; FIELD
Derwent Class: T01
International Patent Class (Additional): **G06F-015/20**
File Segment: EPI

**13/5/11 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


007202855
WPI Acc No: 1987-199864/198729
XRPX Acc No: N87-149621

**Optimising register allocation and assignments method - having source code compiled into executable code in either scalar or vector processor using live variable analysis**

Patent Assignee: IBM CORP (IBMC )

Inventor: MUNSHI A A; SCHIMPF K M
Number of Countries: 014 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 229245 | A | 19870722 | EP 86114964 | A | 19861028 | 198729 | B |
| BR 8605865 | A | 19870825 | | | | 198739 | |
| CN 8607764 | A | 19870701 | | | | 198837 | |
| US 4782444 | A | 19881101 | US 85809989 | A | 19851217 | 198846 | |
| ES 2004348 | A | 19890101 | ES 863326 | A | 19861209 | 198935 | |
| CA 1264859 | A | 19900123 | | | | 199008 | |

Priority Applications (No Type Date): US 85809989 A 19851217
Cited Patents: 5.Jnl.Ref; A3...9012; No-SR.Pub
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 229245 | A | E | 24 | | |
| Designated States (Regional): BE CH DE FR GB IT LI NL SE | | | | | |
| US 4782444 | A | | 8 | | |

Abstract (Basic): EP 229245 A

The source code includes regions of code without **branches** termed 'basic blocks', each having statements defining computations. Each processor comprises memory for storing sequences of executable code and data and device for accessing the memory and executing any accessed code. The memory is mapped as a two-level mode including a finite number of registers P and a comparably infinite internal memory. The registers have access time faster than that of internal memory.

The method involves ascertaining the **data** dependency **graph** attributes of each basic block and generating a local register allocation and assignment for q of the p registers with reference to all computations within each basic block by performing a 'two-colour pebbling game' heuristic over the ascertained **data** dependency **graph** utilising the **two** -level memory **model** .

ADVANTAGE - Minimises the number of spills i.e. the number of references to and from memory

Title Terms: OPTIMUM; REGISTER; ALLOCATE; ASSIGN; METHOD; SOURCE; CODE; COMPILE; EXECUTE; CODE; SCALE; VECTOR; PROCESSOR; LIVE; VARIABLE; ANALYSE
Derwent Class: T01
International Patent Class (Additional): **G06F-009/44** ; **G06F-012/02** ; **G06F-015/40** ; G06I-012/02
File Segment: EPI

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Set      Items   Description
S1       156394   (GRAPH? OR TABLE? OR TUPLE? OR ARRAY? OR MATRIX OR MATRICES
                   OR COLUMN? OR ROW? OR GRID? OR LINE? OR LABEL? OR VALUE? OR -
                 FAT OR MFAT OR NTFS OR VFAT OR (MATHEMATICAL OR DATA)()ELEMEN-
                 T?)(2N)(INFORMATION OR DATA)
S2       270326   NODE? OR TREE? OR SERVER? OR PROCESSOR?
S3        93945   (PAIR OR TWO OR COUPLE OR DUO OR DUAL OR DOUBLE)(2N)(PATTE-
                 RN? OR STRUCTURE? OR MODEL? OR PARAMETER? OR ATTRIBUT? OR FEA-
                 TURE?)
S4       926742   TARGET? OR OBJECT? OR GOAL? OR DESTINATION?
S5       345280   SUBNODE? OR SUB()NODE? OR SUBTREE? OR SUB()TREE? OR CHILD?
                 OR SIBLING? OR OFFSPRING OR OFF()SPRING OR BRANCH? OR LEAVES -
                 OR SLAVE?
S6          406   NODE()RELATIONSHIP()GRAPH? OR NRG
S7       116669   (WALK? OR TEST? ? OR TESTING OR DIAGNOSTIC OR ANALYS? OR A-
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                 OR LOGIC OR EXPRESSION? OR SCHEME? OR TECHNIQUE?)
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S9           12   S6 (S) S7
S10         107   S1 (S) S2 (S) S3 (S) S4 (S) S5
S11           0   S10 (S) S6
S12          65   S10 (S) S7
S13          77   S9 OR S12
S14          34   S13 AND IC=G06F?
S15          13   S14 AND IC=(G06F-007? OR G06F-017?)
File 348:EUROPEAN PATENTS 1978-2004/Sep W01
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040909,UT=20040902
         (c) 2004 WIPO/Univentio
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                T?)(2N)(INFORMATION OR DATA)
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                TURE?)
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                OR SIBLING? OR OFFSPRING OR OFF()SPRING OR BRANCH? OR LEAVES -
                OR SLAVE?
S6         225   NODE()RELATIONSHIP()GRAPH? OR NRG
S7      545864   (WALK? OR TEST? ? OR TESTING OR DIAGNOSTIC OR ANALYS? OR A-
                NALYZ? OR MEASURE? OR INSPECT? OR CHECK? OR VERIFY? OR EXAMIN?
                 OR EVALUAT? OR DETECT?)(2N)(ALGORITHM? OR RULE? OR FORMULA? -
                OR LOGIC OR EXPRESSION? OR SCHEME? OR TECHNIQUE?)
S8           0   S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7
S9          14   S6 AND S7
S10          2   S1 AND S2 AND S3 AND S4 AND S5
S11         39   S1 AND S3 AND S5
S12          2   S11 AND S7
S13         18   S9 OR S10 OR S12
S14          7   S13 NOT PY>2001
S15          7   S14 NOT PD>20011026
S16          7   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/Sep W1
         (c) 2004 Elsevier Eng.  Info. Inc.
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File 202:Info. Sci. & Tech. Abs. 1966-2004/Sep 09
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         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/Aug W3
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Aug
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
```

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9803W3
Abstract: We present a new approach to the placement problem. The proposed approach consists of analyzing the input circuit and deciding on a two-dimensional global grid for that particular input. After determination of the grid size, the placement is carried out in three steps: global placement, detailed placement, and final optimization. We will show that the output of the global placement can also serve as a fast and accurate predictor. Current implementation is based on simulated annealing. We have put all algorithms together in a placement package called **NRG** (pronounced N-er-G). In addition to area minimization, **NRG** can perform timing-driven placement. Experimental results are strong. We improve TimberWolf's results (version 1.2, the commercial version which is suppose to be better than all university versions including version 7) by about 5%. Our predictor can estimate the wirelength within 10-20% accuracy offering 2-20 multiplied by speedup compared with the actual placement algorithm. (Author abstract) 16 Refs.
Descriptors: Computer aided network **analysis** ; **Algorithms** ; Simulated annealing
Identifiers: Global placement; Detailed placement
Classification Codes:
703.1.1 (Electric Network Analysis)
723.5 (Computer Applications); 703.1 (Electric Networks); 921.5 (Optimization Techniques)
723 (Computer Software); 703 (Electric Circuits); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING); 92 (ENGINEERING MATHEMATICS)

**16/5/3 (Item 3 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)


04374285 E.I. No: EIP96023034329
**Title: Multicast** trees **to provide message ordering in mesh networks**
Author: Cordova, Javier; Lee, Yann-Hang
Corporate Source: Univ of Puerto Rico, Arecibo, Puerto Rico
Source: Computer Systems Science and Engineering v 11 n 1 Jan 1996. p 3-13
Publication Year: 1996
CODEN: CSSEEI ISSN: 0267-6192
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9605W5
Abstract: The **objective** of this work is to provide message ordering for mesh networks by constructing multicast **trees** . **Two** different graph **models** can be used to guarantee the message ordering properties. In the first one, a single global **tree** is built for all the **nodes** in overlapping groups, while in the second one, single **trees** are built only for overlapping **nodes** , and on top of these **subtrees** separate **trees** are built for each multicast group. Two problems are investigated to build such **trees** : finding an optimal root that minimizes the time of the multicast, and determining the routing to minimize both time and traffic. An algorithm to find a root **node** that minimizes the time is presented. An efficient heuristic routing algorithm which builds a shortest-path **tree** is also presented. It is shown that this algorithm builds a **tree** whose traffic has an upper bound of twice as much as that of an optimal multicast **tree** . (Author abstract) 6 Refs.
Descriptors: Computer networks; **Data** communication systems; **Graph** theory; **Data** structures; Mathematical models; Data transfer; Algorithms; Heuristic programming; Computational complexity; Optimization
Identifiers: Multicast **trees** ; Message ordering; Mesh networks; Heuristic routing algorithm; Routing
Classification Codes:
722.4 (Digital Computers & Systems); 722.3 (Data Communication, Equipment & Techniques); 921.4 (Combinatorial Mathematics, Includes Graph

Theory, Set Theory); 723.2 (Data Processing); 921.6 (Numerical Methods); 723.1 (Computer Programming)
722 (Computer Hardware); 921 (Applied Mathematics); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

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Set     Items   Description
S1      570374   (GRAPH? OR TABLE? OR TUPLE? OR ARRAY? OR MATRIX OR MATRICES
                  OR COLUMN? OR ROW? OR GRID? OR LINE? OR LABEL? OR VALUE? OR -
                 FAT OR MFAT OR NTFS OR VFAT OR (MATHEMATICAL OR DATA)()ELEMEN-
                 T?)(2N)(INFORMATION OR DATA)
S2     1848094   NODE? OR TREE? OR SERVER? OR PROCESSOR?
S3      158223   (PAIR OR TWO OR COUPLE OR DUO OR DUAL OR DOUBLE)(2N)(PATTE-
                 RN? OR STRUCTURE? OR MODEL? OR PARAMETER? OR ATTRIBUT? OR FEA-
                 TURE?)
S4     4345185   TARGET? OR OBJECT? OR GOAL? OR DESTINATION?
S5     1810520   SUBNODE? OR SUB()NODE? OR SUBTREE? OR SUB()TREE? OR CHILD?
                 OR SIBLING? OR OFFSPRING OR OFF()SPRING OR BRANCH? OR LEAVES -
                 OR SLAVE?
S6        5629   NODE()RELATIONSHIP()GRAPH? OR NRG
S7      114066   (WALK? OR TEST? ? OR TESTING OR DIAGNOSTIC OR ANALYS? OR A-
                 NALYZ? OR MEASURE? OR INSPECT? OR CHECK? OR VERIFY? OR EXAMIN?
                  OR EVALUAT? OR DETECT?)(2N)(ALGORITHM? OR RULE? OR FORMULA? -
                 OR LOGIC OR EXPRESSION? OR SCHEME? OR TECHNIQUE?)
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S9           1   S6 (S) S7
S10          6   S1 (S) S2 (S) S3 (S) S5
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S14         19   S13 NOT PD>20011026
S15         17   RD (unique items)
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S17         12   S16 (S) S1
S18          8   S17 NOT PY>2001
S19          8   S18 NOT PD>20011026
S20          7   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/Sep 13
         (c) 2004 ProQuest Info&Learning
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File 647:CMP  Computer Fulltext 1988-2004/Sep W1
         (c) 2004 CMP Media, LLC
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         (c) 2004 The Dialog Corp.
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         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Sep 13
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Sep 13
         (c) 2004 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2004/Sep 13
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         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Jul
         (c) 2004 The HW Wilson Co
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Set     Items   Description
S1      570374   (GRAPH? OR TABLE? OR TUPLE? OR ARRAY? OR MATRIX OR MATRICES
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                 FAT OR MFAT OR NTFS OR VFAT OR (MATHEMATICAL OR DATA)()ELEMEN-
                 T?)(2N)(INFORMATION OR DATA)
S2     1848094   NODE? OR TREE? OR SERVER? OR PROCESSOR?
S3      158223   (PAIR OR TWO OR COUPLE OR DUO OR DUAL OR DOUBLE)(2N)(PATTE-
                 RN? OR STRUCTURE? OR MODEL? OR PARAMETER? OR ATTRIBUT? OR FEA-
                 TURE?)
S4     4345185   TARGET? OR OBJECT? OR GOAL? OR DESTINATION?
S5     1810520   SUBNODE? OR SUB()NODE? OR SUBTREE? OR SUB()TREE? OR CHILD?
                 OR SIBLING? OR OFFSPRING OR OFF()SPRING OR BRANCH? OR LEAVES -
                 OR SLAVE?
S6        5629   NODE()RELATIONSHIP()GRAPH? OR NRG
S7      114066   (WALK? OR TEST? ? OR TESTING OR DIAGNOSTIC OR ANALYS? OR A-
                 NALYZ? OR MEASURE? OR INSPECT? OR CHECK? OR VERIFY? OR EXAMIN?
                  OR EVALUAT? OR DETECT?)(2N)(ALGORITHM? OR RULE? OR FORMULA? -
                 OR LOGIC OR EXPRESSION? OR SCHEME? OR TECHNIQUE?)
S8           2   S1 (S) S2 (S) S3 (S) S4 (S) S5 (S) S7
S9           1   S6 (S) S7
S10          6   S1 (S) S2 (S) S3 (S) S5
S11         19   S1 (S) S3 (S) S5
S12         20   S8:S11
S13         19   S12 NOT PY>2001
S14         19   S13 NOT PD>20011026
S15         17   RD (unique items)
S16       1654   S5 (S) S7
S17         12   S16 (S) S1
S18          8   S17 NOT PY>2001
S19          8   S18 NOT PD>20011026
S20          7   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/Sep 13
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         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Sep 13
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         (c) 1999 PR Newswire Association Inc
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         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Jul
         (c) 2004 The HW Wilson Co
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**20/5,K/1 (Item 1 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


01501342 01-52330
**USE FORMAT 9 FOR FULL TEXT**
**Key issues in information systems management: An international perspective**
Watson, Richard T; Kelly, Gigi G; Galliers, Robert D; Brancheau, James C
Journal of Management Information Systems: JMIS v13n4 PP: 91-115 Spring 1997 ISSN: 0742-1222 JRNL CODE: JMI
DOC TYPE: Journal article LANGUAGE: English LENGTH: 25 Pages
SPECIAL FEATURE: Charts Appendix References
WORD COUNT: 8551

ABSTRACT: The findings of recent information systems (IS) management studies in ten nations or regions as well as one US multinational study are compared and contrasted. The key concerns of IS executives in these areas, are examined, focusing on identifying and explaining regional similarities and differences. Internationally, there are substantial differences in key issues. Possible reasons for these differences - cultural, economic development, political/legal environment, and technological status - are discussed. It is suggested that national culture and economic development can explain differences in key issues. A revised framework for key issues studies that will more readily support comparison across time and nations is presented.
GEOGRAPHIC NAMES: US

DESCRIPTORS: MIS; Systems management; Economic development; International; Statistical analysis; Comparative studies
CLASSIFICATION CODES: 9190 (CN=United States); 9180 (CN=International); 1130 (CN=Economic theory); 5240 (CN=Software & systems); 9130 (CN=Experimental/Theoretical)

...TEXT: Correspondence Analysis

Correspondence analysis [ 19], a visual data analysis method for contingency tables, is an appropriate statistical **technique** for **analyzing** regional differences when there are few observations (eleven regions) and four independent variables. It is an exploratory technique for displaying the rows (i.e., issues) and columns (i.e., regions) of a **data matrix** as points in one-or two-dimensional space. It decomposes the chi-square measure of association of a table into components in a manner similar to that of principal component analysis for continuous **data** . If two **rows** or columns have similar profiles, their points appear close together in the perceptual map created by correspondence analysis. Correspondence analysis was used by Watson and **Brancheau** [37] to display the relationship between key issues and regions. The ranking of issues was transformed into...

**20/5,K/2 (Item 2 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


01353147 00-04134
**USE FORMAT 9 FOR FULL TEXT**
**Parallel evaluation of software architecture specifications**
Tsai, Jeffery J P; Li, Bing; Juan, Eric Y T
Communications of the ACM v40n1 PP: 83-86 Jan 1997 ISSN: 0001-0782
JRNL CODE: ACM
DOC TYPE: Journal article LANGUAGE: English LENGTH: 4 Pages
SPECIAL FEATURE: Charts References
WORD COUNT: 2755

ABSTRACT: A hybrid parallel evaluation model is presented using a logic-based architecture specification language to speed up processes. A novel parallel evaluation model is presented for a logic-based architecture

specification based on a new static data dependency analysis. This model can preserve maximum parallelism while guaranteeing to generate all the solutions of a logic-based architecture specification without backtracking. The power of this model comes from the fact that the static data dependency is capable of representing all evaluation sequences and all multiple solutions implied by a logic-based architecture specification. The main concepts and principles of the new hybrid model are discussed. In the static data flow analysis step, the multiple evaluation sequences in a log-based architecture specification are found. After the static mode analysis is finished, the system implements the AND-OR parallelism. Based on the analysis of the AND-OR parallelism, there are 2 evaluation models, top-down and bottom-up.

GEOGRAPHIC NAMES: US

DESCRIPTORS: Logic programming; Computer architecture; Models; Distributed processing ; Systems design
CLASSIFICATION CODES: 9190 (CN=United States); 5240 (CN=Software & systems)

...TEXT: a set of clauses. For each clause, the clause head and body are formed by predicates. The **evaluation** of a **logic** -based architecture specification is based on the resolution principle. A **data** **value** is transferred among clauses and within a clause based on the unification **rule** . The **evaluation** of the **logic** -based architecture specification is similar to a depth first search of an AND-OR tree [3, 7...

... of clauses unifiable with a calling predicate are independent of each other. The parallel evaluation of AND- **branches** is much more complex, since it may create binding conflicts during evaluation [5]. An effective and common...

**20/5,K/3 (Item 3 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


00593807 92-08980
**USE FORMAT 9 FOR FULL TEXT**
**A Form-Based Approach for Database Analysis and Design**
Choobineh, Joobin; Mannino, Michael V.; Tseng, Veronica P.
Communications of the ACM v35n2 PP: 108-120 Feb 1992 ISSN: 0001-0782
JRNL CODE: ACM
DOC TYPE: Journal article LANGUAGE: English LENGTH: 13 Pages
SPECIAL FEATURE: Charts Diagrams References
WORD COUNT: 7582

ABSTRACT: An approach to systematically using electronic forms in the database requirements and design processes is described. The basis for the study was a simple form model that includes hierarchically structured forms with an event-driven routing. The Form Definition System provides an inference component to assist an end user with view definitions for their forms where a view definition consists of the hierarchical structure and functional dependencies among form fields. The inference component uses a collection of rules and heuristics along with a purposeful dialogue. An explanation facility provides feedback at several levels of detail. The Expert Database Design System assists a designer in the view integration process. The system provides rules for incrementally integrating the form views and heuristics for mapping the form fields into entity types and relationships. The form-based approach is especially relevant when forms are important in the database and end users are accustomed to form-based work.

GEOGRAPHIC NAMES: US

DESCRIPTORS: Systems design; Data base management; Procedures; Forms; Models; Expert systems; Architecture
CLASSIFICATION CODES: 5240 (CN=Software & systems); 9190 (CN=United States)

...TEXT: TASK where there is a value for MATERIAL.

If two adjacent nodes are not related as parent- **child** , they must be on different paths. The path **detection** **rules** use **information** about missing **values** and node containment to decide that two nodes are oil different paths. Since the Work Order and Job Assignment forms only have a single path, the path **detection** **rules** do not apply.

To decide the parent of node n+1, which lies on a different path...

**20/5,K/4 (Item 4 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


00396166 88-12999
**A Tagless Marking That Is Linear over Subtrees**
Lyon, Gordon
Information Processing Letters v27n1 PP: 23-28 Feb 15, 1988 CODEN: IFPLAT ISSN: 0020-0190 JRNL CODE: IPL
DOC TYPE: Journal article LANGUAGE: English LENGTH: 6 Pages
SPECIAL FEATURE: Diagrams References

ABSTRACT: Garbage collection in a LISP-like environment generally calls for traversing the directed binary **graph** of **data** reachable from a single root to mark all descendent nodes and then sweeping through memory to place all unmarked nodes on a free list. The marking phase, generally a depth-first, left-most traversal, takes time linear in the size of the graph when allowed a stack, extra tag bits, or special address-range conventions. A new algorithm is developed that is a left-most, depth-first marking that uses constant extra space. It has worst-case time but is automatically linear over **subtrees** . The main idea is to delay checking whether a cycle has been encountered as long as possible. This optimistic approach may require undoing some operations made prior to the check, but **subtrees** completely avoid any **checking** . The new **technique** should be particularly suitable for those LISP-like structures that typically acquire relatively few multiple referenced nodes.

DESCRIPTORS: Algorithms; Graphs; LISP ; Mathematical analysis; Computer programming
CLASSIFICATION CODES: 5240 (CN=Software & systems); 9130 (CN=Experimental/Theoretical)

ABSTRACT: Garbage collection in a LISP-like environment generally calls for traversing the directed binary **graph** of **data** reachable from a single root to mark all descendent nodes and then sweeping through memory to place ...

...first marking that uses constant extra space. It has worst-case time but is automatically linear over **subtrees** . The main idea is to delay checking whether a cycle has been encountered as long as possible. This optimistic approach may require undoing some operations made prior to the check, but **subtrees** completely avoid any **checking** . The new **technique** should be particularly suitable for those LISP-like structures that typically acquire relatively few multiple referenced nodes. ...

**20/5,K/5 (Item 1 from file: 636)**
DIALOG(R)File 636:Gale Group Newsletter DB(TM)


04809967 Supplier Number: 66170635 (THIS IS THE FULLTEXT)
**EEMBC 1.0 SCORES, PART 2 : Analysis & Mysteries.**
Levy, Markus
Microprocessor Report, v14, n9, p28

Sept, 2000
ISSN: 0899-9341
Language: English    Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 3157
TEXT:
In the first article of this two-part series (see MPR 8/14/00-01), MDR opened the Pandora's box of the EEMBC benchmarks and examined the finer details of the benchmark scores published on the EEMBC Web site. We presented the processor and compiler vendors with our observations on their products (Table 1). This exploration revealed interesting architectural and compiler differences. Some of these differences were easily explained; some remain a mystery.

Thorough comprehension of the results requires analysis at four overlapping levels. The first level, which was performed by most of the vendors, is a high-level analysis at the benchmark's main function and its relationship to the capabilities of the processor architecture. For example, a benchmark that includes floating-point operations will have the best results on a processor with hardware floating-point capability. However, one would expect even better results on a processor such as NEC's VR5432, which has dual pipelines that let the core execute any combination of integer/integer, integer/FP, or FP/FP instructions. To enable each pipeline to handle both integer and FP operations, NEC split up the FP operations: the fraction goes through the integer portion of the pipe, and the exponent goes through a separate 12-bit ALU. However, this level of analysis provides somewhat of a theoretical guess.

The second level of analysis requires a performance profiling, although it appears that few vendors have done this. Performance profiling would point out the "hot spots" in the benchmark, so that the most important sections of code could be examined. However, a code section may be a "hot spot" for one processor but not necessarily for another. Although this explanation is overly simplified, an example would be a comparison of the execution of a floating-point benchmark on a processor with hardware floating-point support versus a processor that performed floating-point operations in software. Another example might be related to cache size and would depend on the number of cache misses.

This discussion leads to the third, and most timeconsuming, level of analysis, which requires an examination of the compiler's output and resource scheduling to determine how efficiently the processor is being used. For example, does the compiler schedule instructions to adequately take advantage of the processor's dual pipelines? Alternatively, is the processor performing a multiply and add in sequence, or is it able to use its single-cycle MAC operation? Part of a processor's efficiency depends on the type and complexity of the benchmark. A benchmark that lends itself to parallelism will potentially show good results on a superscalar processor. On the other hand, a benchmark that has many consecutive data dependencies will bring that same superscalar processor to its knees.

Another part of understanding a processor's efficiency requires separation of the processor architecture from the compiler, the biggest mystery we have encountered. Most of EEMBC's benchmark results to date have been generated using the "out-of-the-box" method--the source code cannot be altered. This implies that a benchmark score could be far below a processor's potential and therefore, one must carefully examine the compiler's output and resource scheduling. On the other hand, until the vendors run these benchmarks using EEMBC's full-fury (hand-optimized) method, it will be difficult to determine whether the compiler is the processor's limiting factor.

Last is a system-level analysis. Things to look for include cache size and number of cache misses, cache policies (writethrough or write-back), and speed and width of the memory bus. A high-level observation will reveal whether a benchmark and its associated data fit into the caches. For those benchmarks that do not fit into the caches, performance profiling will reveal the number of cache misses and the corresponding benefits or limitations of the memory subsystem.

VRSOOO Floating Point Blows Doors Off Others

For most of the EEMBC automotive/industrial benchmarks, we observed that AMD's 450MHz K6-2 beats out NEC's 250MHz VRSOOO by 40-90%. This is

what we would expect, based on the different clock speeds balanced out with the VR5000's 64-bit architecture and 64-bit external data bus. Additionally, the VR5000's bus is running at 100MHz compared with the K6-2's at 66MHz. But for the floating-point and matrix-arithmetic benchmarks (which are floatingpoint intensive), the K6-2 is 35% and 59% slower, respectively. Another indicator of the VR5000's strong floatingpoint capability appeared when we compared this processor with IBM's 500MHz PowerPC 750CX, which executes three times faster on the benchmarks in this suite, except for the floating-point and matrix-arithmetic benchmarks, where the 750CX was only 1.66 and 2.22 times faster, respectively. A guess may lead one to credit the VR5000's performance on the floating-point capability of the MIPS IV architecture. But we also observed that for the floating-point and matrix math benchmarks, the VR5000 is about 2.5 times faster than NEC's 167MHz VR5432, which is also based on the MIPS IV architecture (the other benchmark scores were fairly close).

In short, the K6 floating-point performance lags the VR5000 because the former is a 32-bit architecture with 32-bitregisters, and FP operations use two instructions to achieve the 64-bit results. In addition, the K6 executes floating-point instructions in a minimum of two processor clocks, whereas the maximum is significantly higher. IBM's 750CX contains a 64-bit FPU that can pipeline up to three instructions. Most of its floating-point instructions execute with three- or fourcycle latency and one- or two-cycle throughput. The VR5432, also with a 64-bit FPU, has many two- to six-cycle latency instructions with one- to five-cycle throughput. A multicycle FPU instruction iterates in the execute stage of the pipeline until it completes, and--since the FPU and CPU instructions share the same issue logic, data path, and pipeline stages--instruction execution stalls. On the other hand, most FPU instructions in the VR5000 have a latency of only two- to fourcycles, with a throughput of one cycle; this performance is caused by the processor's five-stage floating-point pipeline (Figure 1 ).

Poor Floating-Point Performance; Blame the Compiler

In Part 1 we pointed out that Infineon's TriCore superscalar architecture gave the TriCore an average 34% advantage over the 133MHz ElanSC520 for many of the automotive/industrial benchmarks. But the Elan beat the 80MHz TriCore by a factor of only two on the floating-point benchmark, although the TriCore processor performs floating-point operations in software. In general, Infineon said it expected the TriCore to outperform the x86 platform because of TriCore's tuned instruction-set architecture and its cache efficiency, and because it is a multiple-issue machine. However, we expected much better floating-point performance from Elan with hardware support versus TriCore with floating-point emulation.

Since the benchmark results are derived from EEMBC's out-of-the-box method, we shouldn't necessarily assume any architectural deficiencies related to the x86 CPU. However, we still don't know whether to blame Elan's mediocre floatingpoint behavior on the CAD-UL compiler or TriCore's good performance on the hand-coded Tasking library. Tasking's hand-coded library was necessary to take advantage of the pack and unpack instructions that Infineon added to the ISA to accelerate floating-point emulation. CAD-UL claims that it ran its own floating-point benchmarks with its compiler on 486 devices and found no inefficiencies in that area. It also claims that its compiler uses instructions, such as FSIN, as built-in functions, and that it was able to reach better performance than its competitors. Of course, therein lies the problem with nonstandard benchmarks.

The same 80MHz TriCore platform also beat NEC's 143MHz V832 by an average of 23%, except for the FIR filter and IDCT benchmarks, where the V832 was 50% and 12% faster, respectively. Infineon surmises that the 23% better performance is related to TriCore's multi-issue architecture-where it averages an issue rate of 1.5 instructions/clock. Another factor is that this TriCore's caches are four times the size of the V832's caches (16KB versus 4KB), and its memory bus speed has a 1:1 ratio with the core (compared with 3:1 for the V832). In addition, TriCore also has special instructions optimized for control applications; the company claims these instructions help to avoid using a longer sequence of operations to accomplish the same task.

Control applications, which are typically **branch** intensive, often

involve frequent tests on specific bit values. These applications may also perform tests and **branches** on complex combinations of condition flags set in memory, or the program may **branch** according to the relative values of control variables. Although not unique, TriCore supports full relational "compare and **branch** " instructions between two arbitrary **values** in **data** registers. This feature does distinguish it from those architectures that require a separate compare instruction followed by a **branch** on the compare outcome. TriCore's JZ. T and JNZ.T instructions (the T suffix standing for "bit") support direct **branching** on the zero/not-zero values of specific bits in a register. This helps to eliminate shifting and/or masking to isolate a bit value for **branch** control. Furthermore, TriCore's "accumulating logical" and "accumulating compare" instructions can reduce the number of instructions required to **evaluate** complex logical **expressions** by nearly a factor of two. These are three-operand instructions, with one of the operands serving as both the source and the destination for the accumulated logical result. There are accumulating forms for OR as well as AND, combined with all six integer relational compares or with the bit logical operations AND.T, ANDN.T, OR.T, and NOR.T.

Infineon's TriCore runs the automotive benchmarks an average of only 2.8 times faster than Mitsubishi's 40MHz M32R/E. This appears to coincide with processor frequencies, as well as with the dual-issue design of TriCore's architecture. But again, the floating-point benchmark is an exception, because TriCore runs it 20 times faster than the M32R/E. A similar situation exists between the M32R/E and NEC's V832, where the NEC processor is almost nine times faster for floating point. Again pointing to the compiler, we note that the M32R/E using Wind River's Diab compiler seems to deliver poor results; this is the difference between a hand-written floating-point library and one written in C. Mitsubishi claims that its own CC32R compiler yielded almost twice the performance for this benchmark. (However, since the CC32R-related scores are not certified, actual numbers cannot be printed.)

Mitsubishi also published certified scores that allowed MDR to compare the 16MHz M 16C/62A and next-generation 20MHz M 16C/80 16-bit microcontrollers. The newer microcontroller averaged 70% faster, due to an instruction set with more single-cycle execution instructions and 24-bit addressing capability to eliminate the overhead associated with using far pointers. The M 16C/80 allocates one-byte instructions for frequently used 16-bit instructions. Mitsubishi also enhanced the instruction set for 32-bit operations on add, subtract, compare, move, push, and shift instructions.

Windows Handicaps National's 200MHz Geode GX-1

After certifying and publishing its scores for the consumer benchmarks, National realized that its unique benchmarking environment (in which host and target are one) penalized the Geode GX-1's performance. National tried to minimize the Windows overhead by closing all programs and running the benchmark code in DOS mode. However, National's analysis indicated that the results were different if the system booted in safe mode versus DOS mode. Further investigation revealed that the interrupts caused by peripherals (e.g., network card, mouse) and Windows system timer (which controls task switches and the software timers) ate up the benchmark performance. National also noticed that the memory timings of the PC legacy mode were suboptimal, and the integrated graphics unit shared the memory bandwidth. Experiments that are run with interrupts disabled, optimized memory timing, and an add-in graphics card indicate that out-of-the-box scores for the Geode GX1 could be improved 20-75%. Further experiments using alternate compilers proved that Microsoft's MSVC 6.0 compiler limits this processor's performance for these benchmarks.

Nevertheless, the Geode GX-1 was 76-78% faster than the V832 for the JPEG and high-pass filter benchmarks, although it was 21-45% slower for the color-conversion benchmarks. NEC credits the compiler for the V832 results and assumed that the compiler generated code that had fewer memory accesses for the color-conversion benchmarks. NEC also thinks the cache structures are involved.

The write-through cache of the V832 limits its performance on the data-intensive compression and decompression routines. National also pointed out that none of the compilers it tested were able to use the Geode GX-1's MMX instructions; this ability would have allowed the processor to

better handle the extensive number of multiplies integral to the consumer benchmarks.

The high-pass filter benchmark raised another interesting discussion point for NEC's VRS000 when we compared it with the VR5432. Why is the VRS000 20-55% faster for the JPEG and conversion benchmarks but 8% slower for the gray-scale filter? The answer, according to NEC, is that the VRS000's wider bus (64 bits versus 32 bits) and faster bus access (100MHZ versus 83.SMHz) are important for JPEG. On the other hand, the VR5432's integer unit, with its true dual pipeline and greater number of execution units, is 50% faster than that of the VRS000.

The Pipeline Tells the Truth

The Bezier-curve benchmark in the office automation suite also presented the VRS000 (Green Hills compiler) and VR5432 (Apogee compiler) with an interesting challenge. The processor's scores were almost equal, and again this is related to the true dual-pipeline advantage of the VR5432. NEC disabled the compiler optimization for the dual pipeline and discovered that the VR5432's score dropped by almost 40%. As with the gray-scale filter score, the VR5432 beat the VR5000 on the text processing benchmark by 10%. In an experiment with the VRS000, NEC used Apogee's compiler (instead of the one from Green Hills) for the text processing benchmark and was able to beat the VR5432.

Toshiba's 133MHz 32-bit TMPR3927F, also a MIPSbased processor, is 20-40% faster than the V832 for the office automation benchmarks, except for text processing, where it is 12% slower. According to Toshiba, the V832 and TMPR3927 have the same data cache sizes, so the text processing result is proportional to the frequency ratio. However, this is a questionable response, because the V832's cache is write-through, which certainly degrades its performance. (Another factor may be that the TMPR3927's data cache is two-way set-associative compared with the V832's direct-mapped implementation.) Toshiba also believes that the text processing benchmark extensively exercises data transfers and stack manipulations; thus, any additional cache or scratch-pad memory may help improve performance. We don't know whether the compiler can automatically take advantage of the V832's extra 4KB RAM, which could be used for the constants and global variables in the text processing benchmark (this may prevent some cache thrashing).

As for the Bezier-curve and dithering benchmarks, Toshiba has confirmed that the Green Hills compiler takes advantage of the TMPR3927's multiply-accumulate instruction. Again, the verdict is still out on whether the same is true for the V832 and its single-cycle MAC.

Benefits of the Write-Back Cache

In our Part 1 observations with the telecomm benchmarks, we compared the ElanSC520 with IDT's 100MHz 79RC32364 and the V832. We noted that the IDT device was an average of 2.2 times faster than the Elan chip. After looking more closely at the benchmarking setup, we believe that this relationship cannot be attributed to cache sizes, bus speeds, or operating frequency. It's still a mystery whether the CAD-UL compiler (used for the AMD benchmark execution) is or isn't able to extract the full potential out of the SC520, but it's also reasonable to assume that the MiPS-based 79RC32364 is a more efficient architecture for this benchmark. And the benchmark scores improved for the 79RC32364, because IDT discovered that its original scores were derived with the processor's cache in the write-through mode. Two weeks ago, the company sent its platform to ECL (EEMBC Certification Labs) for recertification with the cache in the write-back mode, and the scores increased by up to a factor of two, depending on the benchmark (some telecomm benchmarks did not change appreciably).

We also saw the same trend for IDT with the networking benchmarks. Recertification with the cache in writeback mode demonstrated a 20-40% performance increase, depending on the benchmark. However, the route lookup benchmark scores were identical for write-through and write-back, indicating that this algorithm was more computation intensive than data intensive.

We made another observation for the VR5000 with the Green Hills compiler versus IDT's 79RC64575 with the IDT/c 7.2.1 GNU compiler. Although both processors have the same architecture, the VR5000 ran the OSPF and packet-flow benchmarks (the 512K versions) 36% and 9% faster, respectively.

But, in the other three networking benchmarks, the VRS000 ran 9-18% slower.

Analyzing processors and associated compilers using EEMBC benchmark scores, or any other benchmarks, is a complicated business. This two-part series has helped to expose some intricate architectural details and has raised many questions. Equally important, we persuaded the vendors to look under the hood as they tried to understand how their architectures interacted with the benchmarks.

| Processor Name | Clock rate (MHz) | Compiler | Native Data Type |
|---|---|---|---|
| AMD ElanSC520 | 133 | CAD-UL I381G1X0 | 32 |
| AMD K6-2 | 450 | CAD-UL I381G1X0 | 32 |
| IBM PowerPC 750CX | 500 | Wind River Diab 4.3b | 32 |
| IDT79RC32364 | 100 and 150 | Algorithmics SDE4.0B | 32 |
| IDT79RC64575 | 250 | Algorithmics SDE4.0B | 64 |
| Infineon TriCore TC10GP | 80 | Tasking V1.1r1 | 32 |
| Mitsubishi M16C/62A | 16 | Mitsubishi, NC30, V3.20 R.1 | 16 |
| Mitsubishi M16C/80 | 20 | Mitsubishi NC308WAV2.00 R.1 | 16 |
| Mitsubishi M32R/E | 40 | Wind River Diab Rel4.3 Rev f | 32 |
| National Geode GX-1 | 200 | Microsoft MSVC 6.0 | 32 |
| NEC V832 | 143 | Green Hills V1.8.9 | 32 |
| NEC VR5000 | 250 | Green Hills Multi(r)2000 V2.0 | 64 |
| NEC VR5432 | 167 | Apogee Software V4.1 | 64 |
| Toshiba TMPR3927 | 133 | Green Hills Multi2000 V2.0 | 32 |

| Processor Name | HW FPU | I/D Cache | I/D Cache Type |
|---|---|---|---|
| AMD ElanSC520 | Yes | 16K/16K | 2-way SA |
| AMD K6-2 | Yes | 32K/32K | 2-way SA |
| IBM PowerPC 750CX | Yes | 32K/32K | 8-way SA |
| IDT79RC32364 | No | 8K/2K | 2-way SA |
| IDT79RC64575 | Yes | 32K/32K | 2-way SA |
| Infineon TriCore TC10GP | No | 16K/16K | 2-way SA |
| Mitsubishi M16C/62A | No | n/a | n/a |
| Mitsubishi M16C/80 | No | n/a | n/a |

| | | | |
|---|---|---|---|
| Mitsubishi M32R/E | No | 40K | On-chip RAM |
| National Geode GX-1 | Yes | 16K Unified | 4-way SA |
| NEC V832 | No | 4K/4K (write-through) | Direct-mapped (plus 4k data RAM) |
| NEC VR5000 | Yes | 32K/32K | 2-way SA |
| NEC VR5432 | Yes | 32K/32K | 2-way SA |
| Toshiba TMPR3927 | No | 8K/4K | 2-way SA |

| L2 Cache Processor Name | Bus Clock | Bus Freq. Width | (MHz) |
|---|---|---|---|
| AMD ElanSC520 | n/a | 32 | 66 |
| AMD K6-2 | 66 | 32 | 66 |
| IBM PowerPC 750CX | 500 | 64 | 66 |
| IDT79RC32364 | n/a | 32 | 50 |
| IDT79RC64575 | n/a | 64 | 50 |
| Infineon TriCore TC10GP | n/a | 32 | 80 |
| Mitsubishi M16C/62A | n/a | 16 | 16 |
| Mitsubishi M16C/80 | n/a | 16 | 20 |
| Mitsubishi M32R/E | n/a | 32 | 40 |
| National Geode GX-1 | n/a | 64 | 66 |
| NEC V832 | n/a | 32 | 47.6 |
| NEC VR5000 | 100 | 64 | 100 |
| NEC VR5432 | 100 | 32 | 100 |
| Toshiba TMPR3927 | n/a | 32 | 66 |

Table 1. Comparison of the basic features and compilers of the processors discussed in this article. (n/a = not applicable)


PUBLISHER NAME: Cahners Publishing Company
COMPANY NAMES: *NEC Corp.
INDUSTRY NAMES: BUSN (Any type of business); CMPT (Computers and Office Automation)

... avoid using a longer sequence of operations to accomplish the same task.

Control applications, which are typically **branch** intensive, often involve frequent tests on specific bit values. These applications may also perform tests and **branches** on complex combinations of condition flags set in memory, or the program may **branch** according to the relative values of control variables. Although not unique, TriCore supports full relational "compare and **branch** " instructions between two arbitrary **values** in **data** registers. This feature does distinguish it from those architectures that require a separate compare instruction followed by a **branch** on the compare outcome. TriCore's JZ. T and JNZ.T instructions (the T suffix standing for "bit") support direct **branching** on the zero/not-zero values

of specific bits in a register. This helps to eliminate shifting and/or masking to isolate a bit value for **branch** control. Furthermore, TriCore's "accumulating logical" and "accumulating compare" instructions can reduce the number of instructions required to **evaluate** complex logical **expressions** by nearly a factor of two. These are three-operand instructions, with one of the operands serving...

**20/5,K/7 (Item 1 from file: 160)**
DIALOG(R)File 160:Gale Group PROMT(R)


01751069
**NCR CORPORATION ANNOUNCES 7720-3101 MODULAR ITEM PROCESSING SYSTEM TO SERVE LOW-VOLUME USERS**
News Release July 31, 1987 p. 1

NCR Corporation today introduced a new on-line check processing system that is specifically designed for low volume environments within financial institutions. The NCR 7720-3101 offers rapid document proofing to financial institutions which process 5,000 or fewer document passes daily. The NCR 7720 is designed to help commercial banks, thrifts, and credit unions with lower check volumes avoid the bottlenecks of manual batch processing. Remote **branches** of larger institutions can avoid the risks and delays of courier item delivery by using the NCR 7720 to process the checks at the **branch** rather than at a central location. The NCR 7720-3101 offers single-step item processing, and expedites data handling by allowing users to communicate on- **line** with remote **data** centers for regular account updating. The 7720 System records as many as 100 distributions and 300 totals, encodes with up to 15 line formats, offers five different **check** digit verification **schemes** , and uses intelligent sorting to feed items into one to 12 pockets. Other features include a thermal journal printer and movable PC and proofing keyboards.

Full text available on PTS New Product Announcements.

COMPANY:
*NCR

PRODUCT: *Remittance Processing Systems (3573067)
EVENT: *Product Design & Development (33)
COUNTRY: *United States (1USA)

...banks, thrifts, and credit unions with lower check volumes avoid the bottlenecks of manual batch processing. Remote **branches** of larger institutions can avoid the risks and delays of courier item delivery by using the NCR 7720 to process the checks at the **branch** rather than at a central location. The NCR 7720-3101 offers single-step item processing, and expedites data handling by allowing users to communicate on- **line** with remote **data** centers for regular account updating. The 7720 System records as many as 100 distributions and 300 totals, encodes with up to 15 line formats, offers five different **check** digit verification **schemes** , and uses intelligent sorting to feed items into one to 12 pockets. Other features include a thermal...

```
Set      Items   Description
S1      570374   (GRAPH? OR TABLE? OR TUPLE? OR ARRAY? OR MATRIX OR MATRICES
                  OR COLUMN? OR ROW? OR GRID? OR LINE? OR LABEL? OR VALUE? OR -
                 FAT OR MFAT OR NTFS OR VFAT OR (MATHEMATICAL OR DATA)()ELEMEN-
                 T?)(2N)(INFORMATION OR DATA)
S2     1848094   NODE? OR TREE? OR SERVER? OR PROCESSOR?
S3      158223   (PAIR OR TWO OR COUPLE OR DUO OR DUAL OR DOUBLE)(2N)(PATTE-
                 RN? OR STRUCTURE? OR MODEL? OR PARAMETER? OR ATTRIBUT? OR FEA-
                 TURE?)
S4     4345185   TARGET? OR OBJECT? OR GOAL? OR DESTINATION?
S5     1810520   SUBNODE? OR SUB()NODE? OR SUBTREE? OR SUB()TREE? OR CHILD?
                 OR SIBLING? OR OFFSPRING OR OFF()SPRING OR BRANCH? OR LEAVES -
                 OR SLAVE?
S6        5629   NODE()RELATIONSHIP()GRAPH? OR NRG
S7      114066   (WALK? OR TEST? ? OR TESTING OR DIAGNOSTIC OR ANALYS? OR A-
                 NALYZ? OR MEASURE? OR INSPECT? OR CHECK? OR VERIFY? OR EXAMIN?
                  OR EVALUAT? OR DETECT?)(2N)(ALGORITHM? OR RULE? OR FORMULA? -
                 OR LOGIC OR EXPRESSION? OR SCHEME? OR TECHNIQUE?)
S8           2   S1 (S) S2 (S) S3 (S) S4 (S) S5 (S) S7
S9           1   S6 (S) S7
S10          6   S1 (S) S2 (S) S3 (S) S5
S11         19   S1 (S) S3 (S) S5
S12         20   S8:S11
S13         19   S12 NOT PY>2001
S14         19   S13 NOT PD>20011026
S15         17   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/Sep 13
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/Sep W1
         (c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Sep 10
         (c) 2004 The Dialog Corp.
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Sep 10
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Sep 13
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Sep 13
         (c) 2004 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2004/Sep 13
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Jul
         (c) 2004 The HW Wilson Co
```

01041501 96-90894
**USE FORMAT 9 FOR FULL TEXT**

**Technological support for group process modeling**

Dean, Douglas L; Lee, James D; Orwig, Richard E; Vogel, Douglas R

Journal of Management Information Systems: JMIS v11n3 PP: 43-63 Winter 1994/1995 ISSN: 0742-1222 JRNL CODE: JMI
DOC TYPE: Journal article LANGUAGE: English LENGTH: 21 Pages
SPECIAL FEATURE: Charts References
WORD COUNT: 8209

ABSTRACT: During business analysis, business activities are modeled and analyzed. Redefined models become the blueprints for improved business activities. The cost to produce models of the organization is high and model accuracy is important. Involvement from knowledgeable participants and stakeholders is desirable during business modeling and analysis. Traditional modeling approaches limit direct participation to a small handful of participants. The development and evaluation of an electronic meeting system (EMS) based activity modeling tool are discussed. Modeling efforts supported by this new approach are compared with modeling efforts supported by analysts with a single-user tool. The results of this comparison reveal that the EMS-based modeling tool allows a greater number of individuals to participate efficiently in model development. Models are developed between 175% and 251% faster with the new approach than with the traditional approach. Specific features are discussed that help relatively novice modelers work with analysts to develop models of reasonable quality. Measures are set forth that can be used to assess modeling efficiency and quality.

DESCRIPTORS: Groupware; Systems development; Models; Studies; Statistical analysis
CLASSIFICATION CODES: 5240 (CN=Software & systems); 9130 (CN=Experimental/Theoretical)

...TEXT: the model easily. It is best if these views are generated from semantic data rather than from **data** stored as **graphical** objects. In addition, graphical views should be rich enough to support all important graphical constructs, such as...

... joins, as well as representing tunneled arrow (arrows not balancing explicitly with arrows on the parent or **child** diagrams). Graphical representations of these constructs help reduce cognitive complexity and show where problems exist in the **model** .
**Two** levels of semantic checking support are important. First, at the point of data entry, ICOM attachment should...

... level, such as the mismatch of an input at the parent diagram with its use at the **child** diagram. Two levels of semantic checking provide some initial control, but at the same time allow individuals...

**15/5,K/7 (Item 7 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


00968991 96-18384
**USE FORMAT 9 FOR FULL TEXT**

**The case against CASE**

Martin, Merle P

Journal of Systems Management v46n1 PP: 54-57 Jan/Feb 1995 CODEN: JSYMA9
ISSN: 0022-4839 JRNL CODE: JSM
DOC TYPE: Journal article LANGUAGE: English LENGTH: 4 Pages
SPECIAL FEATURE: References
WORD COUNT: 2402

ABSTRACT: Promises ascribed to computer aided systems engineering (CASE) methodology are many. Among the most predominant are increased productivity, quality, analyst communication, and ease of alteration. There is a marked gap between CASE promises and actual CASE experiences. This gap has at least some of the following dimensions: 1. There is a long learning curve, no less than 6 months and as long as 3 years. 2. Implementation of CASE is as much a change in the firm's culture as ii is an introduction of new technology. 3. CASE is not yet integrated, despite vendor advertising claims. Guidelines are suggested for closing the gap between CASE promises and the current level of CASE experiences, including: 1. Keep expectations realistic. 2. Measure performance. 3. Introduce structured methodology. 4. Emphasize training. 5. Be selective on initial CASE uses. The systems analyst must be more proactive if a complex and costly technological methodology such as CASE is to be sold to management and users.

GEOGRAPHIC NAMES: US

DESCRIPTORS: Computer aided software engineering; Problems; Technological planning; Guidelines
CLASSIFICATION CODES: 5240 (CN=Software & systems); 5220 (CN=Data processing management); 9150 (CN=Guidelines); 9190 (CN=United States)

...TEXT: Flow Diagram (DFD) process and automatically establish an explosion to the next level of refinement. This explosion **feature** accomplishes **two** things. First, the progressively refined explosions are automatically linked together into a **tree** structure for leveling validation and retrieval. Second, relevant **graphic** entities, **data** flows, and data store symbols are automatically copied from the parent to the exploded **child** diagram. This saves analyst symbol generation time.

Code Generation: In many CASE tools, process description at a...

**15/5,K/10 (Item 10 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)


00662433 93-11654
**USE FORMAT 9 FOR FULL TEXT**
**Data resource management for CIM systems: Challenges and design considerations**
Samaddar, Subhashish; Rai, Arun
International Journal of Operations & Production Management v12n11 PP: 42-52 1992 CODEN: IOPMDU ISSN: 0144-3577 JRNL CODE: IJO
DOC TYPE: Journal article LANGUAGE: English LENGTH: 11 Pages
SPECIAL FEATURE: Charts References
WORD COUNT: 4289

ABSTRACT: In any sizeable application of a Computer Integrated Manufacturing (CIM) system, a tremendous amount of complex data needs to be logically integrated and managed. Because of the difficulties associated with managing CIM data, effective data management of such an advanced manufacturing system poses a challenging task for system designers and managers. The difficulty in storing and managing CIM data is mostly due to their heterogeneous characteristics, dynamic nature and entity orientations. Currently available commercial database management systems (DBMS) do not have adequate facilities to maintain or integrate heterogeneous data structures. Also, most DBMSs adhere to a static schema definition. Entity-oriented CIM data cannot be handled by a traditional relational model, which is state of the art in DBMSs. Relational databases offer the most significant potential for achieving a fully integrated system. Though they are not perfectly matched to the problem of managing CIM data, extensions can be made to use them in such an environment.

DESCRIPTORS: CIM; Data base management systems; Manufacturing cells; Relational data bases